User's Manual

RZ/G1E Starter Kit
Board Hardware Manual

YR8A77450HA02BG
(Platform version device)

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Rev.1.00 Dec 2017

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Revision History	RZ/G1E Starter Kit Board Hardware Manual

Rev.	Date of Issue	Description	
		Page	Modification
1.00	Dec, 2017	-	Newly created and released.

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1. Overview

The RZ/G1E is an SOC featuring the basic functionality required for the next generation of display audio systems. Its newly employed bus configuration maximizes the system performance, space saving, and cost efficiency.

The YR8A77450HA02BG board is RZ/G1E-specific evaluation board that can be used to evaluate systems using the RZ/G1E and to develop operating systems, device drivers, and applications. Using the YR8A77450HA02BG board allows the developers to efficiently conduct required tasks such as evaluation of the RZ/G1E system performance and thus greatly to reduce the turn-around time in their product development.

1.1. Features

1.1.1. List of RZ/G1E Functions

- Two 1.0-GHz ARM Cortex™-A7 MPCore™ cores (dual core: option)
- Memory controller for DDR3-SDRAM (DDR3-1333) with 32 bits × 1 channel
- Three-dimensional graphics engines
- Video processing unit
- Sound processing unit
- SD card host interface (3 channels), MMCIF (1 channel)
- USB2.0 host (1 channel), USB2.0 host/function (1 channel)
- DU (digtal RGB 2 channels), VIN (2 channels)
- VSP1, VCP3, FDP1, 2D-DMAC
- SCU, SSIU (10 channels), ADG
- CAN (2 channels), Ethernet MAC
- WDT, TPU, CMT1, TMU, CPG, INTC, DMAC, LBSC
- I^2C (5 channels), IIC (2 channels), SCIF (6 channels), SCIFA (6 channels), SCIFB (3 channels), MSIOF (3 channels), QSPI, HSCIF (3 channels), PWM (7 channels)
- GPIO, etc
- Power supply voltages (typ.) 3.3 V, 1.8 V, 1.5 V/1.35 V, 1.0 V

1.1.2. List of YR8A77450HA02BG Board Functions

Table 1.1.1 Functions of YR8A77450HA02BG Board (1)

YR8A77450HA02BG Board Function List. Page 1 of 2		
Board Function	Module	Description
RAM	DDR3	Single Channel DDR3-1333 1GByte, 32bit data width. 4Gbit(16bit data width) x2 devices.(MT41K256M16 , refer to M2 circuit) SDRAM Backup feature: Not supported.
	LBSC	No device.
ROM	LBSC	Not supported.
	QSPI	SPI Flash: Spansion S25FL512SAGMFIG11 (512Mbit=64MB) x1 device. Spansion S25FL032P0XMFI011 (32Mbit=4MB) x1 device.
Debug I/F	DBG	Connector: HTST-110-01-S-DV (20pin)
	DBG2	through SD card slot for SDHI1
	GPIO	Mechanical switch x3 elements 'TactSW' for Android Purpose.
	SCIFA0	Not supported.
	SCIFA1	Not supported.
	SCIFA2	Debug Serial x1 (TX, RX) USB to UART Bridge SILICON LABS CP2102-GM x1 (Bridge spec: max 1Mbps) Connector: USB Type microAB
LAN	EtherMAC	Debug Ether(100Mbps) RMII PHY: MICREL KSZ8041RNLI Connector: RJ45: TDK TLA-6T718A (Refer to M1 circuit)
		Not supported.
USB2.0 I/F	USB2.0 ch0	USB2.0 Host or Function Connector: Type A.
	USB2.0 ch1	USB2.0 Host Connector: Type A
RTC I/F	I^2C1	Not supported.
SDHI	SDHI0	WiFi module(LBEE6U4ZQC-TEMP) Interface voltage: Either 3.3V or 1.8V.
	SDHI1	Connector: microSD slot.(DM3AT-SF-PEJM5) Interface voltage: 3.3V or 1.8V
	SDHI2	Not supported.
MMC I/F	MMC1	eMMC: micron MTFC8GLWDQ-3M AIT Z x1 device. 8GByte
MSIOF	MSIOF	EXIO connector
HSCIF	HSCIF0	HSCIF0 for WiFi Module

Table 1.1.2 Functions of YR8A77450HA02BG Board (2)

YR8A77450HA02BG Board Function List. Page 2 of 2		
Video Output	DU0	Either [A] or [B] [A] HDMI output HDMI Transmitter. Analog Devices ADV7511WBSWZ(U23) Connector: HDMI standard type A : Tyco 1747981-1 [B] LCD output. Connector: XF2M-4015-1A
	DU1	Analog RGB output DU output format: RGB666.(RGB888 is not supported by the ALT board) Video DAC: Analog Devices ADV7123 (DU1_DOTCLKOUT is connected) Connector: DSUB15pin
Video Input	VIN0	YCbCr 8bit. BT656 Video Decoder: Analog Devices ADV7180WBCP32Z, Connector: RCA
Audio	SSI0, SSI1, SSI2, SSI9	Either [A] or [B] [A] Audio Output(SSI0) or Input(SSI1) Codec: AKM AK4643EN x1 Connector: mini jack x1 for stereo line output Connector: mini jack x1 for stereo line/MIC input [B] Audio Multi-Channel Output.(SSI0, SSI1, SSI2, SSI9) HDMI Transmitter ADV7511WBSWZ Connector: HDMI standard type A
	SSI3, SSI4	SSI for Wi-Fi module
I^2C I/F	I^2C0	Interface voltage: 3.3V Digital LCD panel
	I^2C1	Interface voltage: 3.3V This interface is connected to the following devices. HDMI Transmitter ADV7511, Video decoder ADV7180, Audio codes AK4643, I2C EEPROM
	I^2C2	Not supported.
	I^2C3	Not supported.
	I^2C4	Interface voltage: 3.3V
	I^2C5	Not supported.
	I^2C6	Not supported.
	I^2C7	Interface voltage: 1.8V PowerIC DA9063
WiFi	SDHI0(SDR104) SSI3,4 HSCIF0	LBEE6U4ZQC-TEMP
EXIO Connector	various modules	EXIO Connector 1: Box Wafer 10P 2.0mm EXIO Connector 2: Box Wafer 6P 2.0mm
Power IC	–	Dialog Semiconductor DA9063
Power Supply	–	DC5.0V input
Board size	–	140mm x 120mm

1.2. Usage Notes

1.2.1. YR8A77450HA02BG Board Specifications

- **Take particular care to ensure the correct configurations of the jumpers and switches mounted on the YR8A77450HA02BG board. Incorrect configurations may damage on-board devices.**

- **For the YR8A77450HA02BG board, be sure to use the power supply that comes with it. Applying a voltage greater than 5 V may damage devices on the YR8A77450HA02BG board.**

- **There are sequences for turning on and off the power supply to the RZ/G1E. For the YR8A77450HA02BG board, be sure to obey the notes below.**

  (1) When power is turned on

  Press SW11 once to turn the YR8A77450HA02BG board on

  (2) When power is shut off

  Long press SW11 to turn the YR8A77450HA02BG board off.

1.3. Board Configuration

The YR8A77450HA02BG board is composed of a single board whose size is 140 mm × 120 mm.
Figure 1.3.1 shows a block diagram of the YR8A77450HA02BG board.

1.3.1. Block Diagram of YR8A77450HA02BG Board

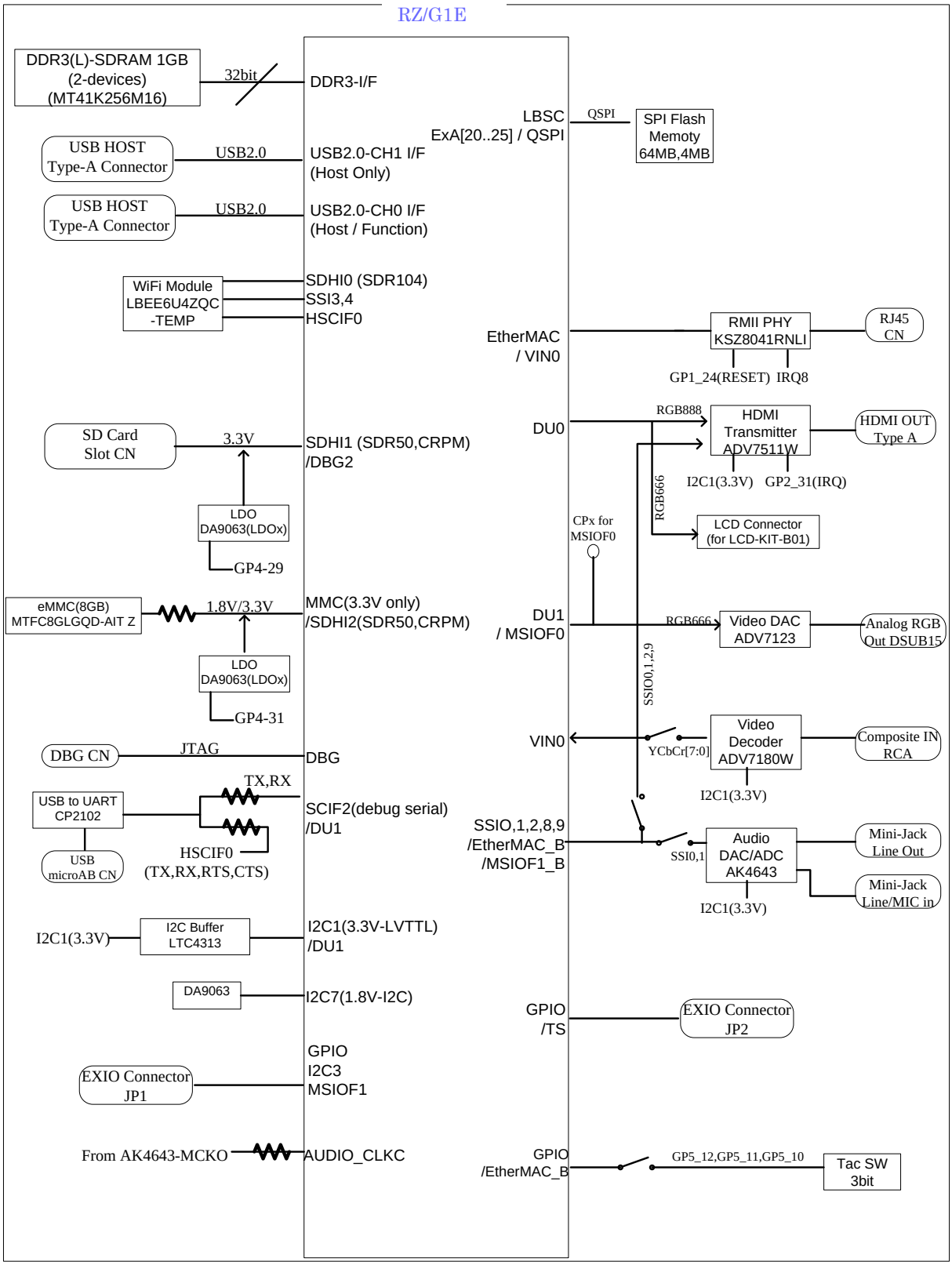


Figure 1.3.1 Block Diagram of YR8A77450HA02BG Board

1.3.2. Address Map of YR8A77450HA02BG Board

For the DDR3L momory space, see the section DDR3-SDRAM Interface.
For the other space, see the RZ/G Series User's Manual: Hardware.

2. YR8A77450HA02BG Interface Module Specifications

2.1. MODE Setting

2.1.1. Specifications

The operating mode of the RZ/G1E is set by a power-on reset. For details on the operating mode, see the documents related to the RZ/G1E operating mode specifications.

2.1.1.1. MD0 Pin — Selection of Free-Running Mode or Step-Up Mode

This pin selects the free-running mode or step-up mode.

MD0	Free-Running Mode or Step-Up Mode
0	Free-running mode
1	Step-up mode

2.1.1.2. MD[3:1] Pins — Selection of Boot Device

These pins select the boot device.

MD3	MD2	MD1	Selection of Boot Device
0	0	0	Boot from area 0 (boot from external mask ROM)
0	1	0	QSPI (48.75 MHz/16-Kbyte transfer)
0	0	1	Reserved
0	1	1	Reserved
1	0	0	QSPI (39 MHz/16-Kbyte transfer)
1	0	1	QSPI (78 MHz/16-Kbyte transfer)
1	1	0	QSPI (39 MHz/4-Kbyte transfer)
1	1	1	Reserved

2.1.1.3. MD4 Pin — Selection of CS0 Space Size

This pin selects whether the area 0 space (CS0) is used as a normal space (64 Mbytes) or an expanded space (128 Mbytes).

MD4	Area Division
0	Area 0: 64 Mbytes
1	Area 0: 128 Mbytes

2.1.1.4. MD5 Pin — Reserved

Do not change the initial setting at shipment (MD5 = 1).

2.1.1.5. MD[7:6] Pins — Selection of Master Boot Processor

These pins select the master boot processor.

MD7	MD6	Selection of Master Boot Processor
0	0	Setting prohibited
0	1	CA7 boot
1	0	SH boot (32 bits)
1	1	Setting prohibited

2.1.1.6. MD8 Pin — Selection of Area 0 Space Data Bus Width

This pin sets the data bus width of the area 0 space (CS0) to 8 bits or 16 bits. Select the data bus width of the boot device connected to the LBSC.

MD8	EXBUS Area 0 Data Bus Width
0	8-bit bus
1	16-bit bus

2.1.1.7. MD9 Pin — Selection of Crystal Resonator or Crystal Oscillator

This pin selects either a crystal resonator or a crystal oscillator to be connected to the EXTAL/XTAL pins. A crystal oscillator (X5: 20 MHz) is mounted on the YR8A77450HA02BG board by default.

MD9	EXTAL/XTAL Pin Setting
0	An external clock is input to the EXTAL pin.
1	A crystal resonator is connected to the EXTAL and XTAL pins.

2.1.1.8. MD12 — Reserved

Do not change the initial setting at shipment (MD12 = 0).

2.1.1.9. MD21, MD20, MD11, MD10, and MDT[1:0] Pins — Switching of JTAG, SDHI1, and SDHI2

These pins select the debugging function through the JTAG connector (CN1) or the SD card slot for the SDHI1 (CN4). The debugging through the SDHI1 or SDHI2 is possible by the combination of MD pin settings in the RZ/G1E specifications.

MD10	MD[21:20]	MD11	MDT[1:0]	JTAG	SDHI1	SDHI2
0	00	-	--	Boundary SCAN	Normal function	Normal function
0	10	0	--	Coresight*	Normal function	Normal function
0	10	1	00	Coresight*	Audio DSP	Normal function
0	10	1	01	Coresight*	SH-X4	Normal function
0	10	1	10	Coresight*	Normal function	Audio DSP
0	10	1	11	Coresight*	Normal function	SH-X4
0	11	0	--	SH-X4	Normal function	Normal function
0	11	1	00	SH-X4	Coresight (*1)	Normal function
1	01	0	--	Coresight*	Normal function	Normal function
1	01	1	01	Coresight*	SH-X4	Normal function

Note: * “Coresight” is an abbreviation of “Coresight debug port”.

2.1.1.10. MD[14:13] Pins — Frequency Mode Setting

These pins select the frequency mode. A crystal oscillator (X5: 20 MHz) is mounted on the YR8A77450HA02BG board.
Do not change the initial setting at shipment (MD14 = 0, MD13 = 1).

MD14	MD13	EXTAL Frequency	EXTAL Divider	PLL1 (CPGM main)	PLL0 (CPGMC)	PLL3 DDR3-1333 MD19 = 1
0	0	15 MHz	× 1/1	× 208 VCO = 3120 MHz	x200 VCO = 3000MHz	× 88 VCO = 1320 MHz
0	1	20 MHz	× 1/1	× 156 VCO = 3120 MHz	x150 VCO = 3000MHz	× 66 VCO = 1320 MHz
1	0	26 MHz	× 1/2	× 240 VCO = 3120 MHz	x230 VCO = 2990MHz	× 102 VCO = 1326 MHz
1	1	30 MHz	× 1/2	× 208 VCO = 3120 MHz	x200 VCO = 3000MHz	× 88 VCO = 1320 MHz

2.1.1.11. MD18 Pin — Reserved

Do not change the initial setting at shipment (MD18 = 0).

2.1.1.12. MD19 Pin — Selection of DDR3-SDRAM Bus Clock

This pin selects the frequency of the DDR3-SDRAM bus clock. Do not change the initial setting at shipment (MD19 = 1).

MD19	Switching of DDR Clock
0	Setting prohibited.
1	DDR3-1333 mode

2.1.2. Initial Values of Mode Setting Pins on YR8A77450HA02BG Board

Table 2.1.1 Initial Values of RZ/G1E Mode Setting Pins on YR8A77450HA02BG Board

MD Pins	Initial Value	Initial Function
MD0	0	Free-running mode
MD[3:1]	101	Boot from the QSPI (78 MHz/16-Kbyte transfer)
MD4	0	Area 0 space size (64 Mbytes)
MD5	1	—
MD[7:6]	01	Cortex-A7 boot
MD8	0	Area 0 space data bus width (16 bits)
MD9	0	Crystal oscillator is used.
MD12	0	—
MD10, MD[21:20], MD11, MDT[1:0]	0,00,0,00	JTAG (CN1) = Boundary SCAN SDHI1 and SDHI2 = Normal function
MD[14:13]	01	Input frequency = 20 MHz
MD18	0	—
MD19	1	DDR3-1333 mode

2.1.3. Multiplexing and Method of Setting for Mode Setting Pins

The following table covers the pin functions that are multiplexed with the mode pins of the RZ/G1E, and how the individual mode pins are set.
For the mode pins that are used with fixed values, resistors are used to set them to their fixed values according to the initial settings in Table 2.1.1, Initial Values of RZ/G1E Mode Setting Pins on YR8A77450HA02BG Board. Such mode pins are described as "Fixed by a resistor" in the Setting Method column in the table below.

Table 2.1.2 Pin Multiplexing of Mode Setting Pins of RZ/G1E

Pin Name	Pin Function	Strapping Options	How to Set	Default Setting
MD0	A1	0: Free-running mode 1: Step-up mode	Fixed by a resistor	ON (0)
MD1	A4	Selects boot device	Fixed by a resistor	OFF (1)
MD2	A3			ON (0)
MD3	A0			OFF (1)
MD4	A7	Selects area-0 size	Fixed by a resistor	ON (0)
MD5	A9	-	Fixed by a resistor	OFF (1)
MD6	A13	Selects boot processor	Fixed by a resistor	OFF (1)
MD7	A15			ON (0)
MD8	BS#	Selects EXBUS data bus width	Fixed by a resistor	Pulled-down (0)
MD9	GP1_20	EXTAL or EXTAL/XTAL	Fixed by a resistor	Pulled-down (0)
MD10	DU0_DSIP	Debugging mode	Fixed by a resistor	ON (0)
MD11	DU0_HSYNC			ON (0)
MD12	DU0_VSYNC	-	Fixed by a resistor	ON (0)
MD13	GP2_31	Selects frequency mode	Fixed by a resistor	Pulled-up (1)
MD14	RD#			ON (0)
MD18	A19	-		ON (0)
MD19	WE0#	DDR clock mode	Set by SW7	OFF (1)
MD20	WE1#	Debugging mode	Fixed by a resistor	ON (0)
MD21	GP1_25		Set by SW7	OFF (1)
MDT0	A18	Debugging mode	Fixed by a resistor	ON (0)
MDT1	A2			ON (0)

2.1.4. Block Diagram of Peripheral Circuit for Mode Pins

On the YR8A77450HA02BG board, pull-up (100 kΩ) and pull-down (10 kΩ) resistors are used to implement the settings of the mode pins that are largely used with fixed values. When changes to the settings of mode pins are likely, this can be implemented by switches which, through resistive voltage division, select the low level when turned on and the high level when turned off.
When the RZ/G1E is released from the power-on reset (when the PRESET# signal of the RZ/G1E is changed from low to high), the mode value set by the switch or resistive voltage division is input to the RZ/G1E.

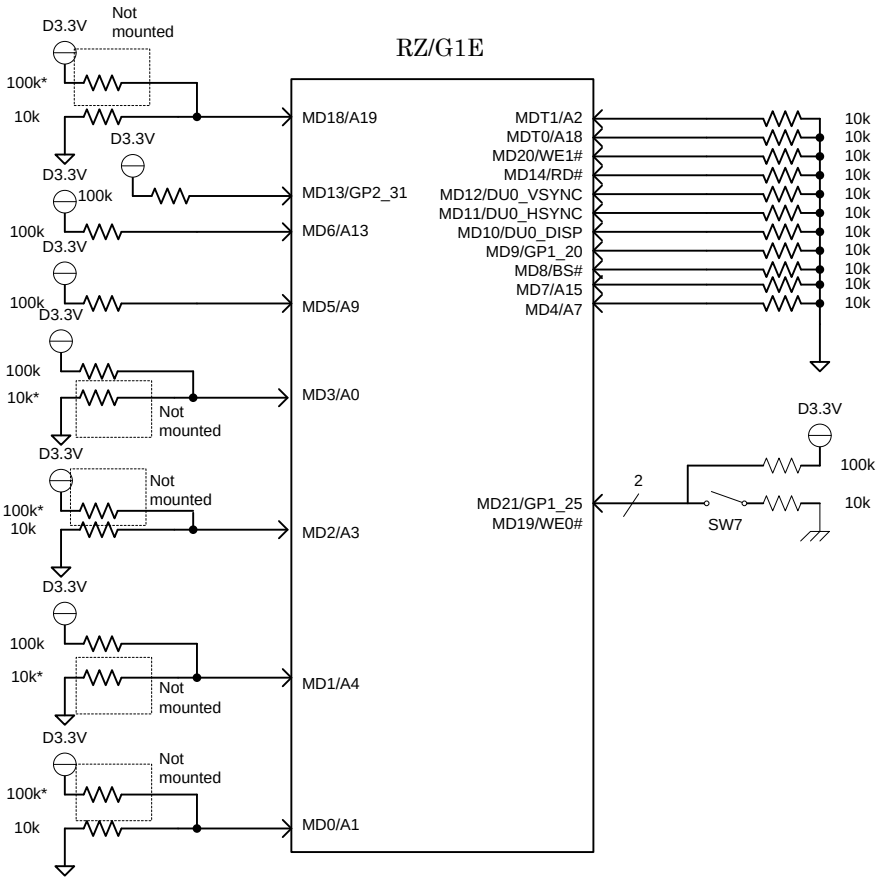


Figure 2.1.1 Peripheral Circuit for Mode Pins on YR8A77450HA02BG Board

DDR3-SDRAM Interface

2.2.1. Specifications

The YR8A77450HA02BG board incorporates two 4-Gbit DDR3-SDRAMs (16-bit bus width) and operates at a maximum speed of DDR3-1333.
The DDR3-SDRAMs are allocated to the address space from H'01_0000 0000 to H'01_FFFF FFFF in the RZ/G1E. The address ranges from H'00_4000 0000 to H'00_BFFF FFFF can be accessed by default as a mirror area of H'01_0000 0000 to H'01_7FFF FFFF.

Table 2.2.1 DDR3-SDRAM Specifications

Interface	DDR3-SDRAM
Product name	MT41K256M16HA-125 AIT:E (DDR3-1600, ×16 bits, 4 Gbits) × 2 pcs
Power supply voltage	1.50 V
Capacity	Total: 1 Gbyte, H'01_0000 0000 to H'01_3FFF FFFF
Bus width	32-bit data bus
Memory bus frequency (RZ/G1E spec.)	DDR3-1333 max.

2.2.2. Signal Correlation

Table 2.2.2 DDR3-SDRAM Signal Correlation

RZ/G1E	DDR3-SDRAM (M1) D[31:16]	DDR3-SDRAM (M2) D[15:0]	Notes
M0DQ[31:16]	DQU[7:0], DQL[7:0]	—	
M0DQ[15:0]	—	DQU[7:0], DQL[7:0]	
M0A[15:0]	A[15:0]	←	
M0BA[2:0]	BA[2:0]	←	
M0CK1, M0CK1#	—	–	Not connected
M0CK0, M0CK0#	CK, CK#	←	
M0CKE1	—	–	Not connected
M0CKE0	CKE	←	
M0CS1#	—	–	Not connected
M0CS0#	CS#	←	
M0WE#	WE#	←	
M0RAS#	RAS#	←	
M0CAS#	CAS#	←	
M0DQS3, M0DQS3#	DQSU, DQSU#	—	
M0DQS2, M0DQS2#	DQSL, DQSL#	—	
M0DQS1, M0DQS1#	—	DQSU, DQSU#	
M0DQS0, M0DQS0#	—	DQSL, DQSL#	
M0DM3, M0DM2	DMU, DML	—	
M0DM1, M0DM0	—	DMU, DML	
M0ODT1	—	—	Not connected
M0ODT0	ODT	←	
M0RESET#	RESET#	←	

Note: Half voltage of VDDQ_M0 is supplied to the M0VREFDQ[1:0] pins of the RZ/G1E.

2.2.3. Block Diagram

The following figure shows a block diagram of the DDR3-SDRAM interface.

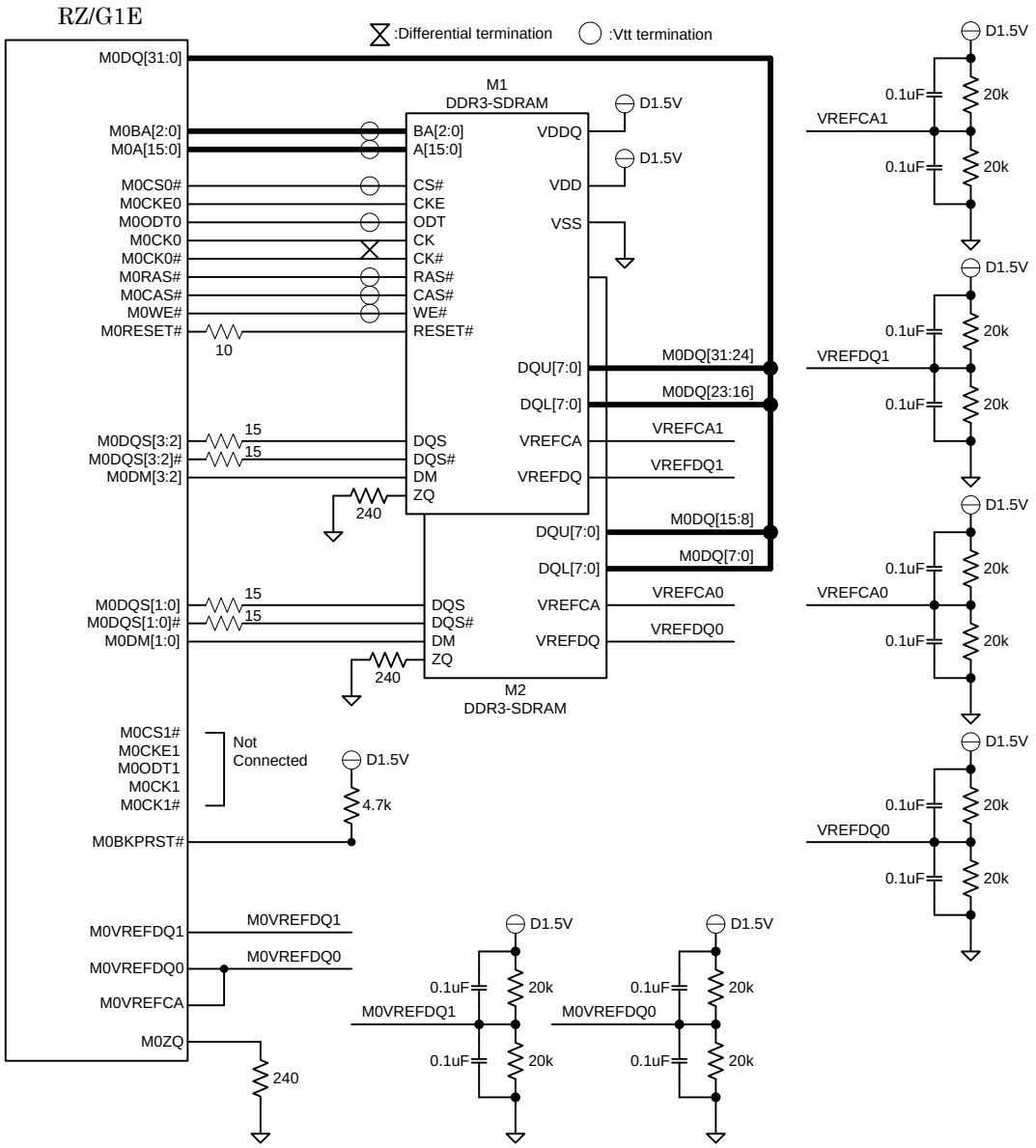


Figure 2.2.1 Block Diagram of DDR3-SDRAM Interface

2.3. SPI-FLASH Interface (QSPI)

2.3.1. Specifications

The YR8A77450HA02BG board incorporates 512-Mbit and 32-Mbit SPI flash memory devices manufactured by Spansion. These SPI flash memory devices are connected to the QSPI of the RZ/G1E via switches SW9. When the 512-Mbit SPI flash memory (U6) is to be accessed, set SW9 to pin 1 side, and when the 32-Mbit SPI flash memory (U7) is to be accessed, set SW9 to the pin 3 side.

Since the loader and mini-monitor are stored in the lower-order address space of the SPI flash memory (U7, 32 Mbits), do not modify the contents of this area. The contents of the SPI flash memory (U6, 512 Mbits) can be modified as required.

Table 2.3.1 SPI-FLASH Interface Specifications

QSPI controller	RZ/G1E's on-chip QSPI module
SPI flash memory	(1) U6: Spansion S25FL512SAGMFIG11 (512 Mbits) (2) U7: Spansion S25FL032P0XMFI011 (32 Mbits)
Clock rate of RZ/G1E's QSPI	78-MHz operation (max.)

2.3.2. Block Diagram

A block diagram of the SPI flash memory interface is shown below.

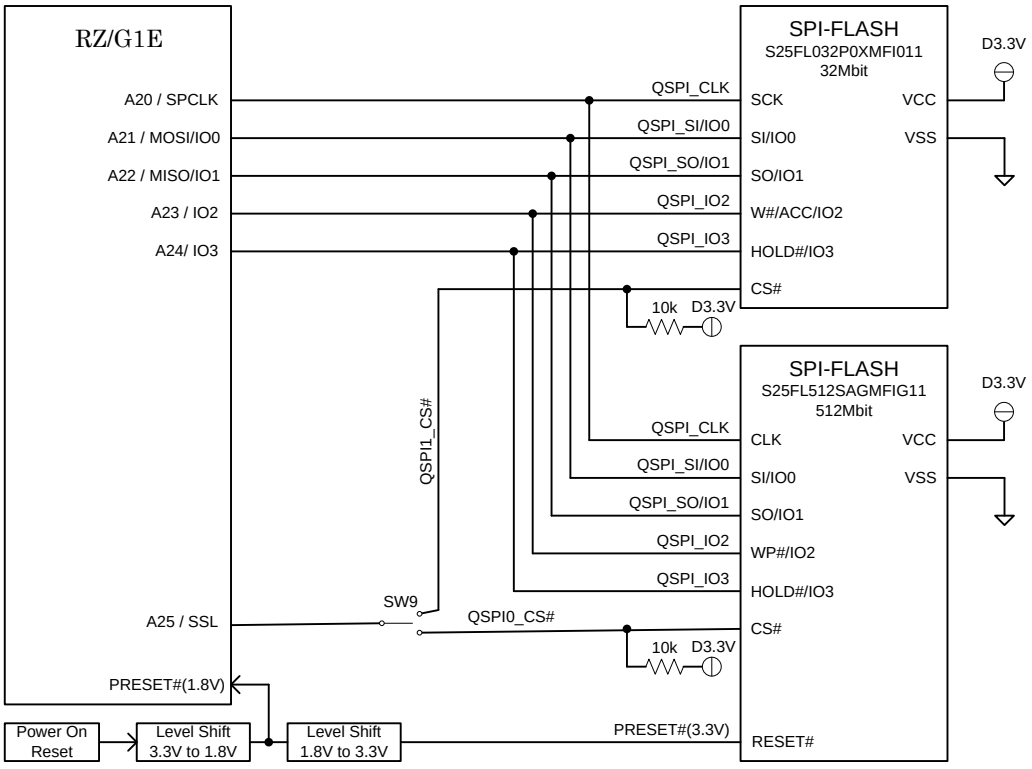


Figure 2.3.1 Block Diagram of SPI-Flash Interface

2.4. Video Input Interface (VIN0)

2.4.1. Specifications

The RZ/G1E has two video input interfaces (VIN0 and VIN1). For details of these functions, see the section on video input in the RZ/G Series User's Manual: Hardware.

On the YR8A77450HA02BG board, ADV7180WBCP32Z (U21) manufactured by Analog Devices is connected to VIN0 of the RZ/G1E and used as a composite video decoder. The ADV7180WBCP32Z (U21) handles inputs in the ITU-R BT.656 8-bit (YCbCr) format. The registers of ADV7180 can be set via an I²C interface (channel 1) of the RZ/G1E.

The block diagram of the VIN0 is shown below.

2.4.2. Block Diagram

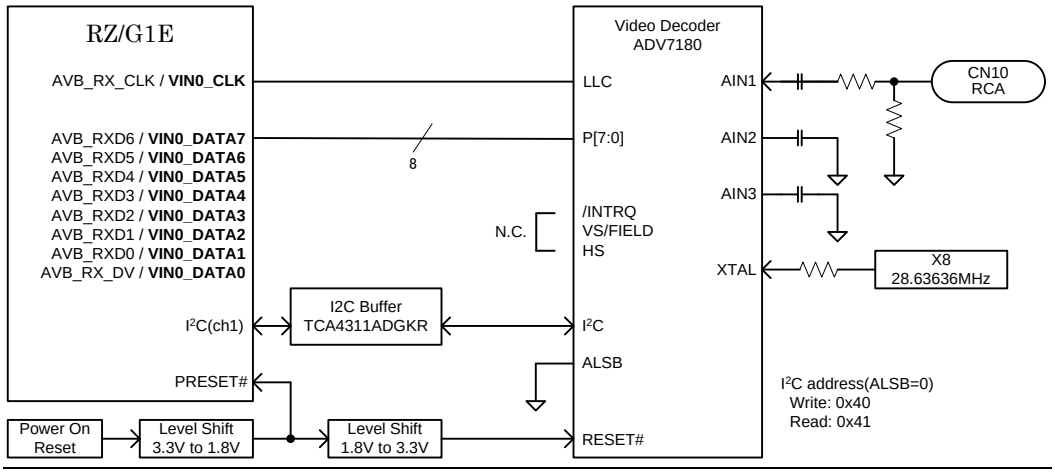


Figure 2.4.1 Block Diagram of Video Input Interface (VIN0)

2.5. Video Output Interface

2.5.1. Specifications

The RZ/G1E incorporates two display units (DU0 and DU1) with the digital RGB interface.

The YR8A77450HA02BG board incorporates an HDMI transmitter (ADV7511), an Digital LCD connector, and a video D/A converter (ADV7123). The respective devices convert the digital RGB signals (RGB888) from DU0 to HDMI signals and digital RGB signals (RGB666) from DU1to analog RGB signals.

The internal registers of the HDMI transmitter (ADV7511) are accessible via an I^2C interface (channel 1) of the RZ/G1E. The INT output is connected to the GP2_31 pin of the RZ/G1E.

On the YR8A77450HA02BG board, the external dot clock inputs are connected as follows: DU0_DOTCLKIN is connected to X2 (148.50 MHz) and DU1_DOTCLKIN is connected to X3 (74.25 MHz, socket-mounted). Alternatively, a clock signal derived by frequency-dividing the RZ/G1E's internal clock can be selected. For details, see the display unit specifications in the RZ/G Series User's Manual: Hardware.

Table 2.5.1 Video Output Interface Specifications

Display controller	RZ/G1E's on-chip display unit (DU)
DU0 (digital RGB, RGB888)	[HDMI Output] HDMI transmitter converts digital RGB signals to HDMI signals. U15: ADV7511WBSWZ by Analog Devices I^2C slave address: 0x72 for write, 0x73 for read. Interrupt: GP5_23 Connector CN6: HMNF-195N-4BH90 (HDMI type A, standard, 19-pin) [LCD Output] Touch pannel connector, for panel with part name "LCD-KIT-B01" Connector CN8: FPC-VI-FPC-05L
DU1 (digital RGB, RGB666)	[Analog RGB Output] Video D/A converter converts digital RGB signals to analog RGB signals. U18: ADV7123KSTZ140 by Analog Devices Connector CN9: D02-M15SAG-23L9E by JAE

2.5.2. Block Diagram

A block diagram of the video output interface on the YR8A77450HA02BG board is shown below.

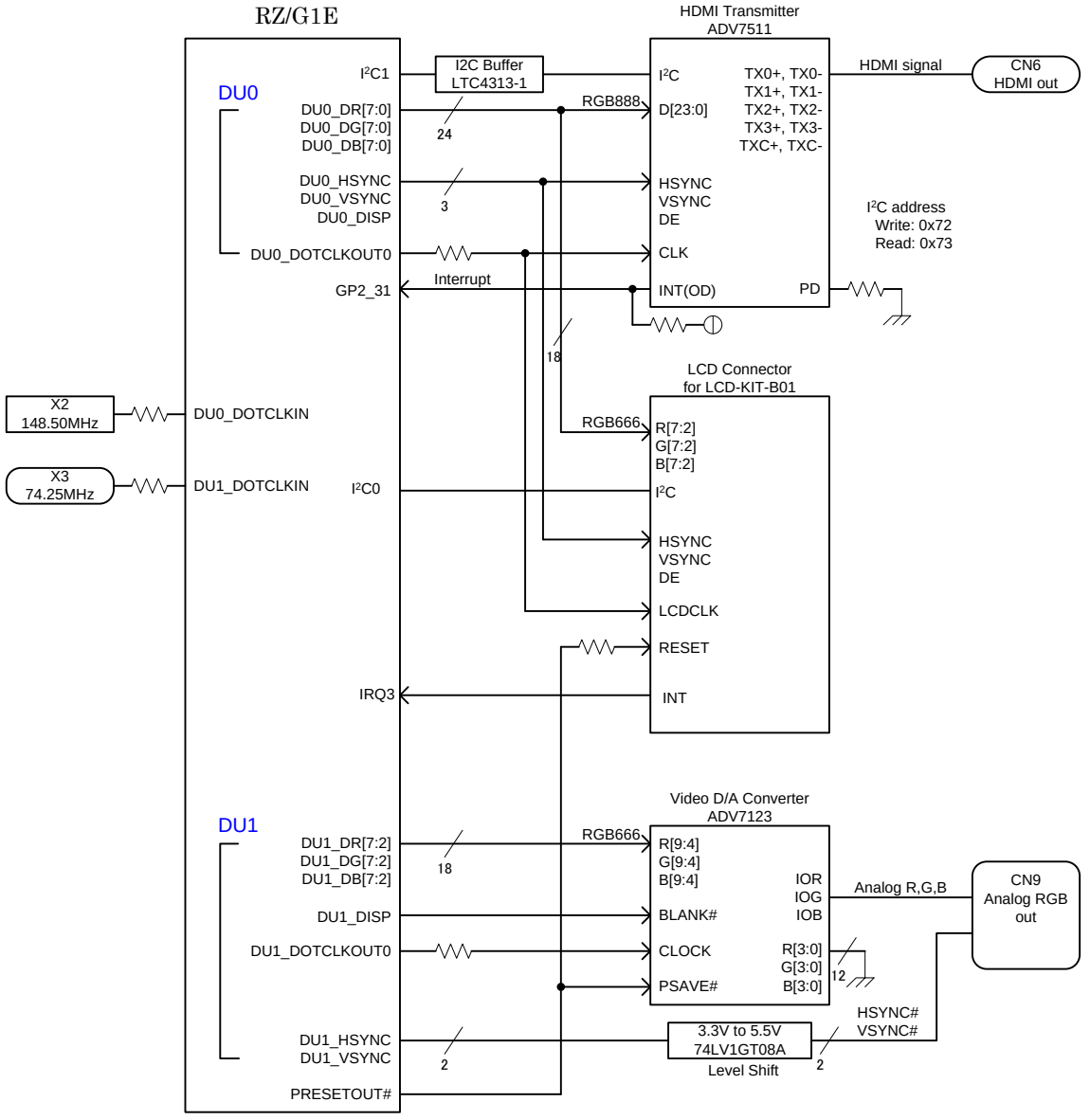


Figure 2.5.1 Block Diagram of Video Output Interface

2.6. Debugger Interface

2.6.1. Specifications

The YR8A77450HA02BG board incorporates two debugger interfaces; one is a 20-pin connector (DBG) for connection to the JTAG emulator.
The RZ/G1E supports the DBG2 and DBG3 interface as a debugger interface, but the YR8A77450HA02BG board does not include this function. For details on the debugger interface, see the RZ/G Series User's Manual: Hardware.

Table 2.6.1 Specifications of DBG and DBG2

DBG interface (20-pin)	CN1: HTST-110-01-S-V by Samtec

2.6.2. Block Diagram

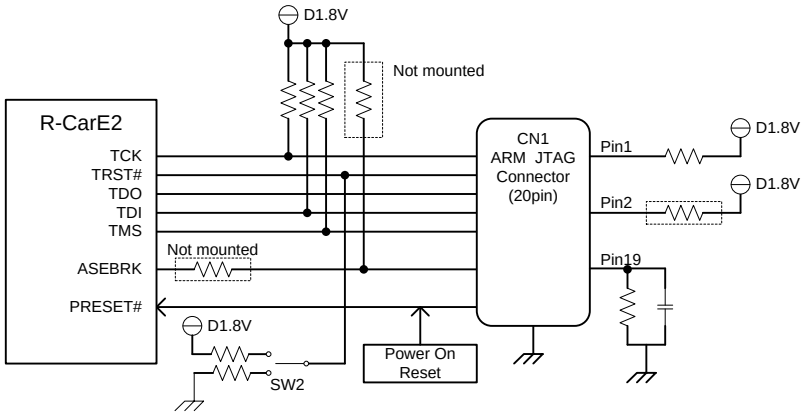


Figure 2.6.1 Block Diagram of JTAG Interface (DBG)

2.7. Debug Ether Interface (EtherMAC)

2.7.1. Specifications

The RZ/G1E incorporates one Ethernet MAC that supports 100 Mbps or 10 Mbps and is compliant with IEEE 802.3u.
On the YR8A77450HA02BG board, the signals for the MAC, EtherMAC or EtherMAC_B, are connected to the RMII PHY interface (KSZ8041RNLI) manufactured by Micrel.
The pin functions for the EtherMAC and Ethernet AVB are multiplexed on the same pins due to the specifications of the RZ/G1E's pin function controller. Accordingly, the EtherMAC and Ethernet AVB functions cannot be used at the same time. When the Ethernet AVB function and EtherMAC PHY function of the YR8A77450HA02BG board are to be used at the same time, use the EtherMAC_B function, since the Ethernet AVB and EtherMAC_B functions can be used at the same time.

Table 2.7.1 Debug Ether Interface Specifications

MAC Layer	RZ/G1E's on-chip EtherMAC and EtherMAC_B
Physical Layer Transceiver	U13: KSZ8041RNLI (RMII) by Micrel
Reset method	Assertion of RESET# (GP1_24 = '0') Negation of RESET # (GP1_24 = '1')
Interrupt request	IRQ8#
Modular Connector	CN5: CWKRJ-13BNL

2.7.2. Block Diagram

A block diagram of the debug Ether interface is shown below.

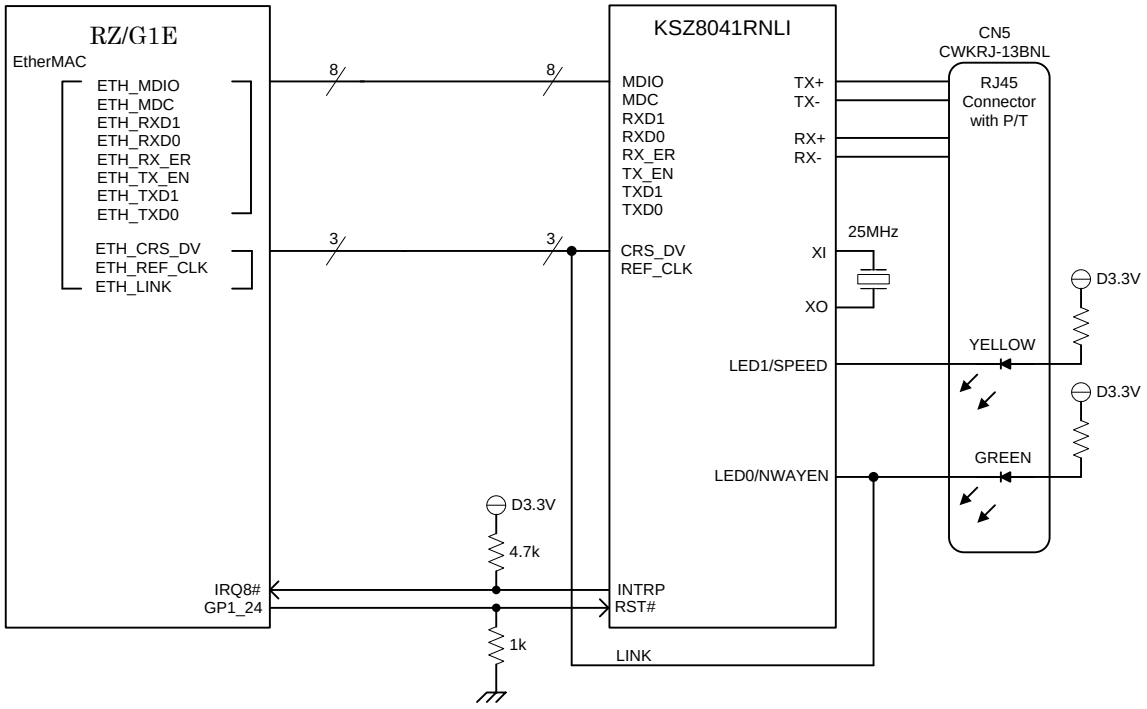


Figure 2.7.1 Block Diagram of Debug Ether Interface

2.8. Audio Codec Interfaces (SSI0, SSI1, SSI2, and SSI9)

2.8.1. Specifications

On the YR8A77450HA02BG board, the codec (AK4643) is connected to the SSI0 and SSI1 of the RZ/G1E. The reset signal PRESETIN# input to the RZ/G1E is level-shifted to 3.3 V and connected to the power-down (PDN) pin of the AK4643.
The audio interface of AK4643 is in the slave mode after PRESETIN# is released from a reset and can be switched to the master mode by a register that is accessed via the I²C interface 1. Furthermore, the SSI on the RZ/G1E side can be set as the master or a slave. It is assumed that SSI_SDATA0 is set to transmit mode and SSI_SDATA1 is set to receive mode on the YR8A77450HA02BG board.
Among the signals of the audio interface, the signals of SSI0, SSI1, SSI2, and SSI9 are also connected to HDMI transmitter ADV7511 (U15) on the YR8A77450HA02BG board. For the connections between the RZ/G1E and each device, see Table 2.8.2.
The pin functions for the SSI_SDATA1, SSI_SDATA2 and EtherMAC_B are multiplexed on the same pin due to the specifications of the RZ/G1E's pin function controller. Accordingly, the SSI_SDATA1, SSI_SDATA2 functions and EtherMAC_B function cannot be used at the same time.

Table 2.8.1 SSI Codec Specifications

Controller	RZ/G1E's on-chip SSI0 and SSI1
Codec	U22: AK4643EN by Asahi Kasei
Audio interface	RZ/G1E (SSI) = Master or slave selectable AK4643EN = Master or slave selectable (default: slave)
Audio connector	LINE-OUT(CN11, 3.5-mm mini-jack) LINE-IN/MIC-IN (CN12, 3.5-mm mini-jack)

2.8.2. Block Diagram

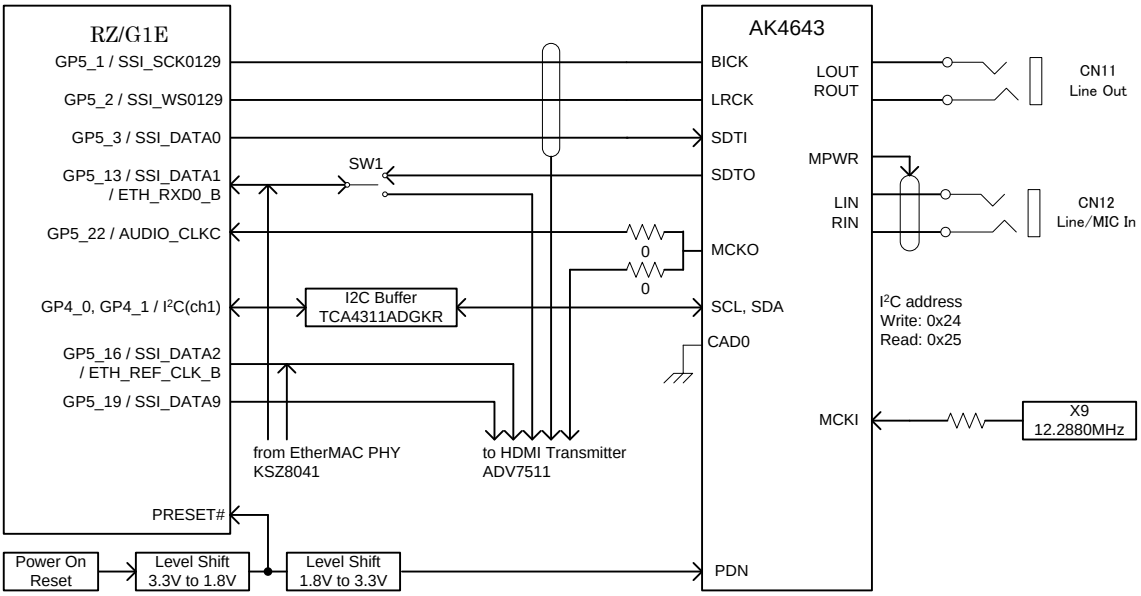


Figure 2.8.1 Block Diagram of Audio Codec

Table 2.8.2 SSI Connections on the YR8A77450HA02BG board

RZ/G1E		AK4643	ADV7511
GP5_22	AUDIO_CLKC	Connected (0-Ω resistors are mounted).	Connected (0-Ω resistors are mounted).
GP5_1	SSI_SCK0129	—	—
GP5_2	SSI_WS0129	—	—
GP5_3	SSI_SDATA0	—	—
GP5_13	SSI_SDATA1	Connected (SW1).	Connected (SW1).
GP5_16	SSI_SDATA2	—	—
GP5_19	SSI_SDATA9	—	—

2.9. SD Card Host Interface (SDHI1)

2.9.1. Specifications

The YR8A77450HA02BG board incorporates an SD card slot (CN4) for the on-chip SD card host interface (SDHI1) of the RZ/G1E. For details on the SDHI1, see the RZ/G Series User's Manual: Hardware.
On the YR8A77450HA02BG board, the power (3.3 V) to be supplied to the VDD pin (pin 4 of CN4) of the SD card slot can be controlled by GP4_26. When GP4_26 is set to 1, power is supplied. When GP4_26 is set to 0, power is shut off.

Table 2.9.1 SD Card Host Interface (SDHI1) Specifications

SD card host interface	RZ/G1E's on-chip SD card host interface 1 (SDHI1)
Voltage control for VDD (pin 4 of CN4)	VDD (pin 4 of CN4) = 3.3 V (GP4_26 = '1') VDD (pin 4 of CN4) = 0.0 V (GP4_26 = '0')
Control of power supply voltage for the SDHI1 interface	VCCQ_SD2 = 3.3 V
SD card slot	MSPN09-A0-1002 (CN4)

2.9.2. Block Diagram

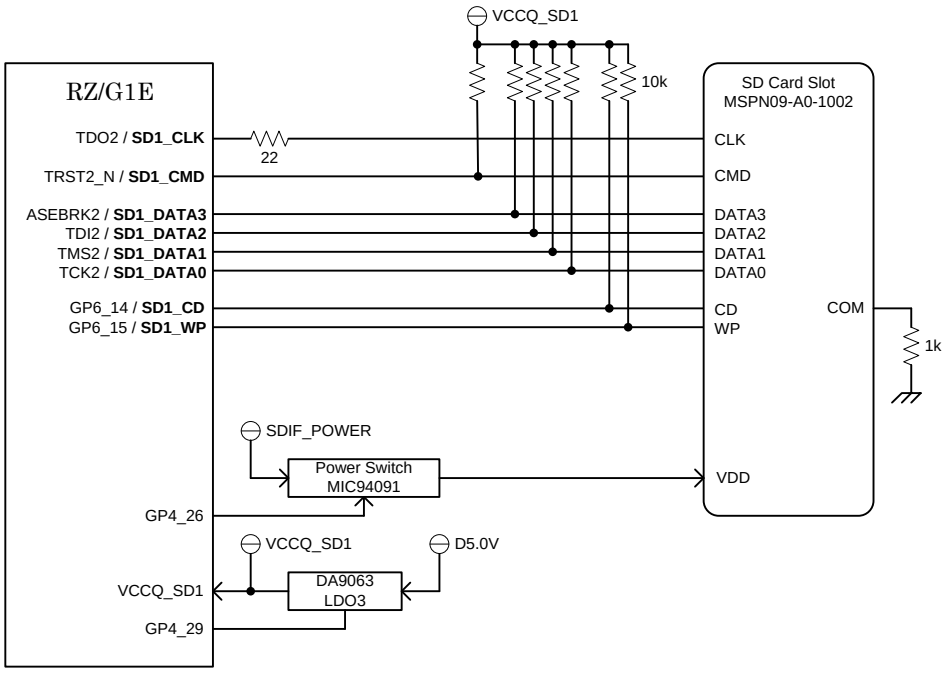


Figure 2.9.1 Block Diagram of SD Card Host Interface (SDHI1)

2.10. eMMC Memory Interface (MMC)

2.10.1. Specifications

The YR8A77450HA02BG board incorporates an eMMC memory MTFC8GLWDQ-3M AIT Z (8 GB, U5) manufactured by Micron that is connected to the on-chip MMC interface of the RZ/G1E. For details on the MMC, see the RZ/G Series User's Manual: Hardware.

Only 3.3 V can be supplied as the power supply voltage for the MMC interface (as VCCQ_SD2) due to the specifications of the RZ/G1E's MMC. Accordingly, be sure to set the GP4_31 pin to 1 when the eMMC memory (U5) on the YR8A77450HA02BG board is to be used.

Table 2.10.1 eMMC Memory (MMC) Interface Specifications

MMC controller	RZ/G1E's on-chip MMC interface (MMC)
Power supply voltage for the MMC interface	VCCQ_SD1 = 3.3 V
eMMC memory	U5: MTFC8GLWDQ-3M AIT Z (8 Gbytes)

2.10.2. Block Diagram

A block diagram of the eMMC memory interface is shown below.

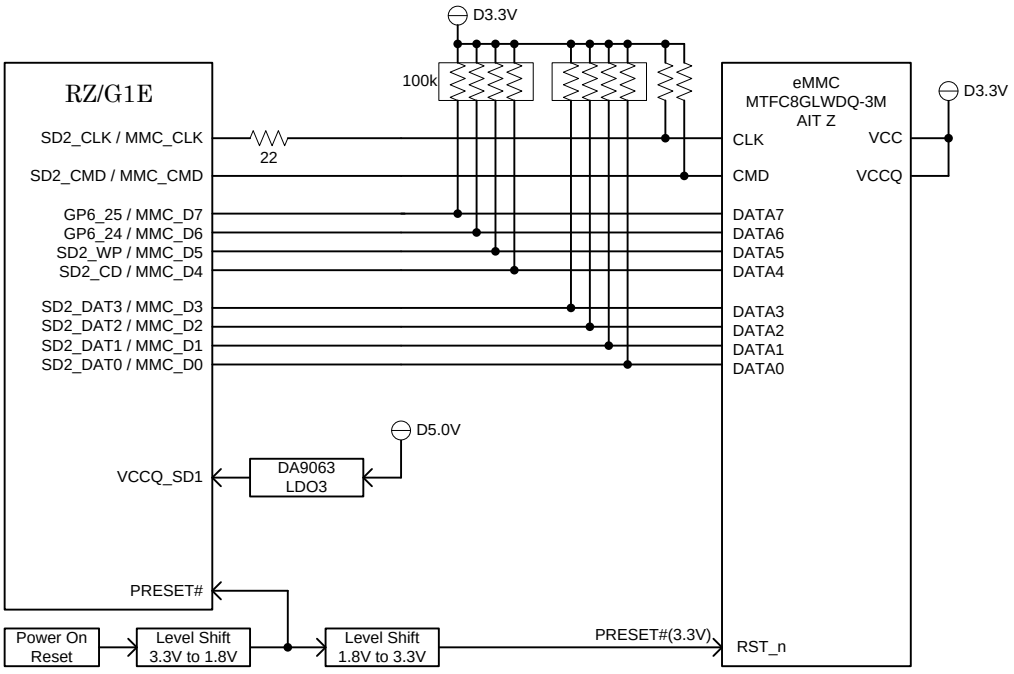


Figure 2.10.1 Block Diagram of eMMC Memory Interface

2.11. USB2.0 Interface

2.11.1. Specifications

The YR8A77450HA02BG board has two USB2.0 ports that can be used as two USB2.0 host interface ports or one USB2.0 host interface port and one USB2.0 function interface port. The function interface is supported in channel 0. The YR8A77450HA02BG board incorporates a a type A connector as CN2. For details on USB2.0, see the USB specifications in the RZ/G Series User's Manual: Hardware and related datasheets.

Table 2.11.1 USB2.0 Specifications

USB controller	RZ/G1E's on-chip USB2.0 host and function controller
USB power supply	BD82065FVJ by ROHM Current limit 2.4 [A]
USB host CN	RZ/G1E USB CH1 CN2 type A connector USB-A x2 lower side
USB host/function CN	RZ/G1E USB CH0 CN2 type A connector USB-A x2 upper side
ESD protection diode	HZD6.2Z4 by Renesas
Common mode filter	DLM11SN900HY2 by Murata
Chip beads	BLM18PG330SN1D by Murata

Note: The connector for channel 0 of the USB in the RZ/G1E is a type A connector shared by the USB host and function.

2.11.2. Block Diagram

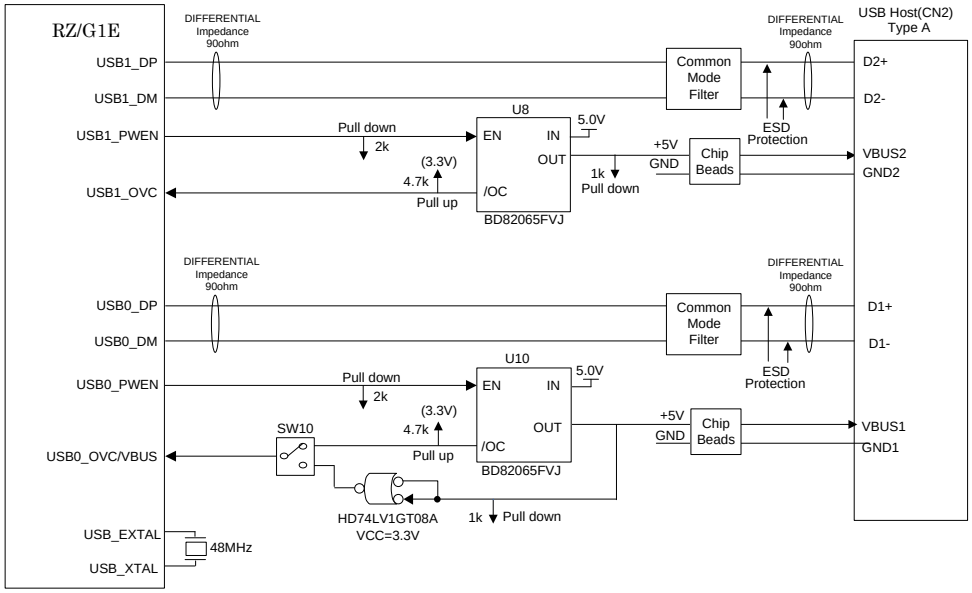


Figure 2.11.1 Block Diagram of USB2.0

2.12. Debug Serial Interface (SCIF2)

2.12.1. Specifications

On the YR8A77450HA02BG board, the SCIF2 of the RZ/G1E is used as a debug serial interface. The SCIF2 of the RZ/G1E is connected to the USB micro-AB connector (CN4) via the USB to UART bridge CP2102. By connecting CN4 to the host PC through USB cable, this interface can be used as a debug serial interface.
The SCIF_CLK pin of the RZ/G1E is connected to the 14.7456-MHz crystal oscillator (X4) on the YR8A77450HA02BG board, which supplies a clock frequency of 14.7456 MHz. When 14.7456 MHz is the frequency of the source clock, since the UART supports 300 bps to 1 Mbps due to the CP2102 device specifications, the maximum transfer rate becomes 921.6 kbps, which is obtained by dividing the source clock by 16. The SCIF2 has the features shown below. For details, see the SCIF specifications in the RZ/G Series User's Manual: Hardware.

- Asynchronous serial communications
- Full-duplex communication supported
- Selectable bit rates by using the RZ/G1E's on-chip baud-rate generator

The host PC connected to the YR8A77450HA02BG board requires the CP2102 USB driver software. This driver software can be obtained from the following URL.
http://www.silabs.com/products/mcu/Pages/USBtoUARTBridgeVCPDrivers.aspx

Table 2.12.1 Debug Serial Interface Specifications

Serial controller	RZ/G1E's on-chip SCIF2 controller
USB to UART bridge	CP2102 (1 Mbps max.) by Silicon Laboratories
Connector	CN13: KS-MCR-B02T3-L

2.12.2. Block Diagram

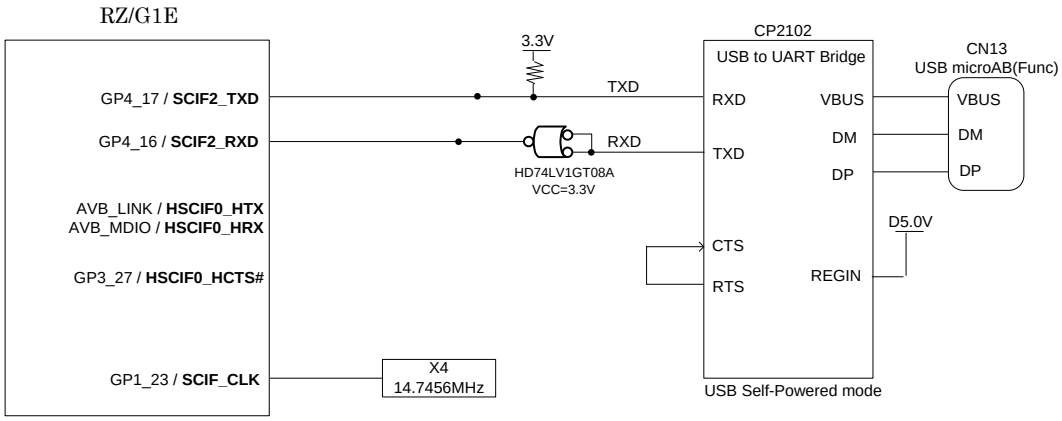


Figure 2.12.1 Block Diagram of Debug Serial Interface

2.13. Reset

2.13.1. Specifications

In the YR8A77450HA02BG board specifications, the power-on reset signal is cleared by the reset IC MAX708SCSA, 200 ms after the 3.3-V power supply has settled. The power supplies for other voltage levels, 12.0 V, 5.0 V, 1.8 V, 1.5 V, and 1.0 V, are not monitored.
A power-on reset signal can be generated by pushing the push switch (SW5). The reset signal is level-shifted from 3.3 V to 1.8 V by the HD74ALVC1G07 and is input to the PRESET# pin of the RZ/G1E.

Table 2.13.1 RESET Specification

Reset IC	MAXIM MAX708SCSA - Threshold voltage: 2.93 V - Reset delay time: 200 ms

2.13.2. Block Diagram

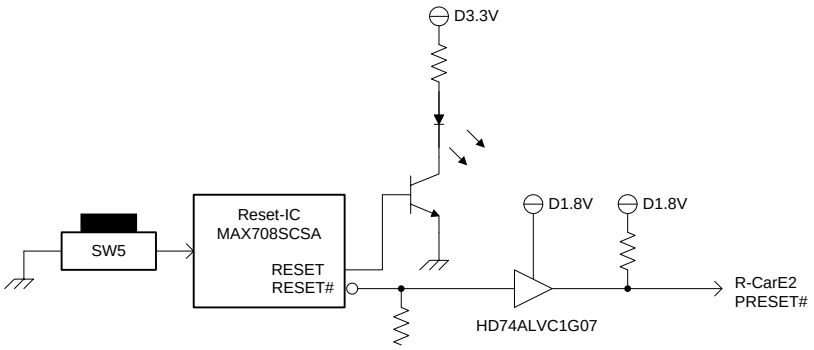


Figure 2.13.1 Block Diagram of Reset Circuit

2.14. I²C Interface

2.14.1. Specifications

The RZ/G1E has eight I²C interface channels. Channel 7 is a 1.8-V interface and channels 0 to 6 are 3.3 V interfaces.
Since the RZ/G1E uses LVTTL-type I/O buffers on I²C interfaces 1, it cannot directly drive an I²C bus with a relatively high load capacitance (e.g. 100 pF).
While the above restriction applies to interfaces 1 of the RZ/G1E, the design of the YR8A77450HA02BG board calls for multiple I²C devices being connected to I²C interfaces 1. In order to compensate for the driving ability of the RZ/G1E, the YR8A77450HA02BG board incorporates an TCA4311ADGKR I²C buffer manufactured by Texsa Instruments, via which each I²C device is connected to the I²C interface for the device.
The following devices are connected to each I²C interface on the YR8A77450HA02BG board.

Table 2.14.1 I²C Interface Specifications

I²C controller	RZ/G1E's on-chip I²C controller
I²C devices through I²C (channel 7)	[1.8 V] U30: Pins B4 (SK) and A5 (SI) of DA9063 by Dialog Semiconductor
I²C devices through I²C (channel 4)	[3.3 V] U17: TestIC (not mounted)
I²C devices through I²C (channel 3)	[3.3 V] JP1: EXIO
I²C devices through I²C (channel 1)	[3.3 V] U15: ADV7511WBSWZ by Analog Devices U21: ADV7180WBCP32Z by Analog Devices U22: AK4643EN by AKM Semiconductor U30: Pins A8 (CLK) and A7 (DATA) of DA9063 by Dialog Semiconductor U14: R1EX24002ATAS0 by Renesas
I²C devices through I²C (channel 0)	[3.3 V] CN8: LCD-KIT-B01

2.14.2. List of Slave Addresses

The table below lists the slave addresses of the I²C devices on the YR8A77450HA02BG board.

Table 2.14.2 List of I²C Slave Addresses

I²C channel	Ux CNx	Device		SA7	SA6	SA5	SA4	SA3	SA2	SA1	R/W#	Note
7	U30	DA9063	PMIC	-	-	-	-	-	-	-	-	-
4	U17	TestIC	Connector	-	-	-	-	-	-	-	-	Not mounted
3	JP1	EXIO										-
1	U15	ADV7511	HDMI Tx	0	1	1	1	0	0	1	X	Pin 22 (PD/AD) = GND
	U21	ADV7180	Video decoder	0	1	0	0	0	0	0	X	Pin 26 (ALSB) = GND
	U22	AK4643	SSI codec	0	0	1	0	0	1	0	X	Pin 8 (CAD0) = GND
	U30	DA9063	PMIC	-	-	-	-	-	-	-	-	-
	U14	R1EX24002	I2C EEPROM	1	0	1	0	0	0	0	X	Pins 3 to 1 (A[2:0]) = GND
0	CN8	LCD-KIT-B01	Connector									

2.14.3. Block Diagram

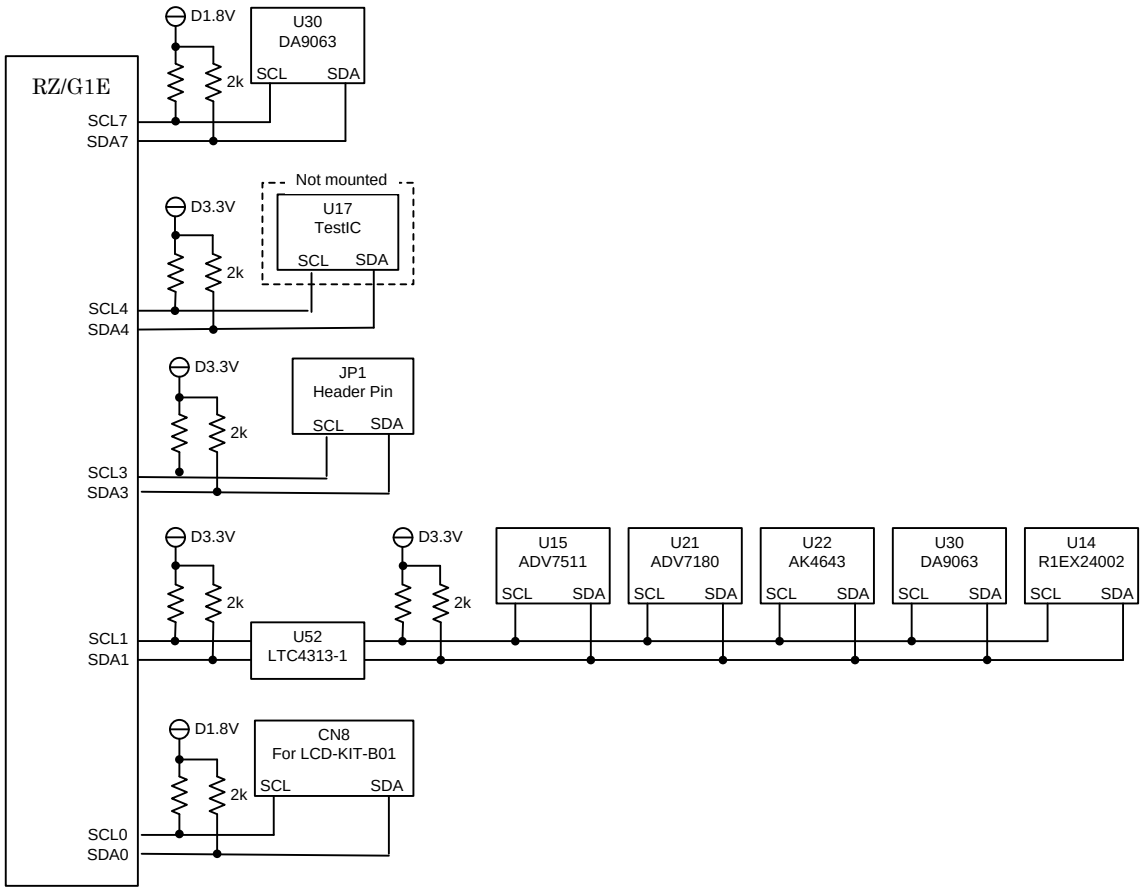


Figure 2.14.1 Block Diagram of I²C Interface

2.15. GPIO Interface (Software Switch, Tact Switch)

2.15.1. Specifications

The YR8A77450HA02BG board incorporates a 4-bit software switch (SW12), three bits of tactile switches (SW3, SW4, SW6) They are connected to the GPIO pins of the RZ/G1E as follows.
When the software switches are to be used, enable the internal pull-up resistors for GP3_12, GP3_11, GP3_10, and GP3_9.

Table 2.15.1 List of Software Switches (General-Purpose Switches)

Software Switch	GPIO	Multiplexed Function
Bit 3 (Pin 4 of SW12)	GP3_12	AVB_TX_EN
Bit 2 (Pin 3 of SW12)	GP3_11	AVB_COL
Bit 1 (Pin 2 of SW12)	GP3_10	AVB_RX_ER
Bit 0 (Pin 1 of SW12)	GP3_9	AVB_RXD7

Table 2.15.2 List of Tactile Switches (General-Purpose Switches)

Tact Switch	GPIO	Multiplexed Function
Bit 2 (SW6)	GP5_12	ETH_RX_ER_B
Bit 1 (SW4)	GP5_11	ETH_CRS_DV_B
Bit 0 (SW3)	GP5_10	IRQ9 / ETH_MDIO_B

2.15.2. Block Diagram

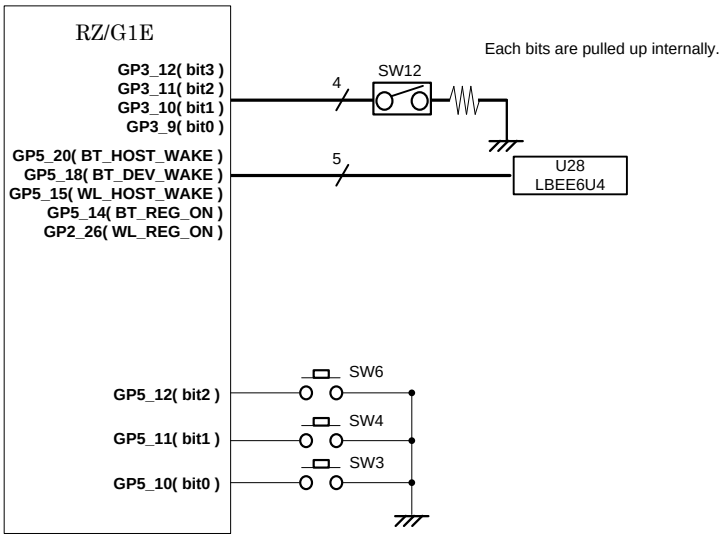


Figure 2.15.1 Block Diagram of GPIO Interface (Software Switch, Tactile Switches)

2.16.

2.16. External Interrupts

2.16.1. Specifications

The RZ/G1E has external interrupt input pins NMI and IRQ[9:0].
The YR8A77450HA02BG board uses NMI and IRQ8 as external interrupt input pins, and GP3_31, and GP5_23 as GPIO interrupts. These pins should be used as active-low signals in programs.
For the interrupt functions of the RZ/G1E, see the RZ/G Series User's Manual: Hardware.
The devices and connectors of the interrupt request sources on the YR8A77450HA02BG board are shown below.

Table 2.16.1 External Interrupt Specifications

Interrupt Pin	Devices that Output Interrupt Request	Connectors
NMI	Pull high	-
IRQ8	RMII PHY U13: KSZ8041RNLI by Micrel	-
GP3_31	PMIC U30: DA9063 by Dialog Semiconductor	-
GP5_23	HDMI transmitter U15: ADV7511WBSWZ by Analog Devices	-

2.16.2. Block Diagram

A block diagram of external interrupts is shown below.

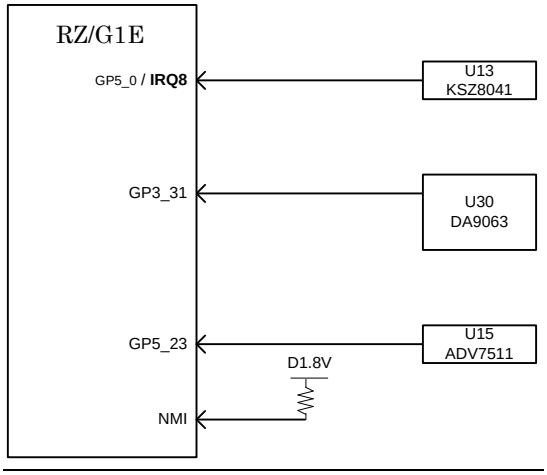


Figure 2.16.1 Block Diagram of External Interrupts

2.17. Clock

The YR8A77450HA02BG board uses the crystal oscillators and resonators shown below.

2.17.1. Clocks Supplied to the RZ/G1E

Table 2.17.1 List of Clocks and Crystals for RZ/G1E

No.	Xn	Frequency	Pin Name on RZ/G1E	Type	Remarks
1	X1	48.0000 MHz	USB_XTAL, USB_EXTAL	Resonator	-
2	X3	74.25 MHz	DU1_DOTCLKIN	Oscillator	-
3	X2	148.500 MHz	DU0_DOTCLKIN	Oscillator	-
4	X4	14.7456 MHz	SCIF_CLK	Oscillator	-
5	X5	20.0000 MHz	EXTAL	Oscillator	
6	X10	32.768 KHz	LPO_IN	Oscillator	-

2.17.2. Clocks Supplied to Devices Other than RZ/G1E

Table 2.17.2 List of Clocks and Crystals Other than for RZ/G1E

No.	Xn	Frequency	Device	Device Pin Name	Type
1	X6	25.0000 MHz	KSZ8041RNLI	XI, XO	Resonator
2	X7	12.0000 MHz	ADV7511WBSWZ	CEC_CLK	Oscillator
3	X8	28.63636 MHz	ADV7180WBCP32Z	XTAL	Oscillator
4	X9	12.2880 MHz	AK4643	MCKI	Oscillator
5	X11	32.768 kHz	DA9063	XTAL_IN, XTAL_OUT	Resonator
6	X10	32.768 kHz	LBEE6U4XQC-DTEMP	LPO_IN	Oscillator

2.18. Power Supply

2.18.1. Specifications

The YR8A77450HA02BG board operates on a single 5.0-VDC power supply.
The power supplies used for the YR8A77450HA02BG board are generated by the switching regulators and low-dropout regulators.
Take care to ensure the following two points:

(1) Specified sequences should be used to turn on and off the power supply to the RZ/G1E. Be sure to control the Power switch (SW11, press once to power on, long press to power down) to obey the power sequence on the YR8A77450HA02BG board.

See the table below for regulators used to generate power supplies on the YR8A77450HA02BG board, their input voltage (Vin) and output voltage (Vout), and whether the Power switch can be used to enable or disable output of power supplies.

Table 2.18.1 List of Switching Controllers and Regulators on the YR8A77450HA02BG Board

Vin	Vout	Switching Controller/Regulator	Power MOSFET	Power Switch Control
Power Supply DC5.0V through CN14	D5.0V	-	-	Not supported
D5.0V	D1.0V	Dialog Semiconductor DA9063 (U30)	-	Supported
	D1.5V	Dialog Semiconductor DA9063 (U30)		Supported
	D3.3V	Dialog Semiconductor DA9063 (U30)	-	Supported
	VTT	Dialog Semiconductor DA9063 (U30)	-	Supported
	D1.8V	Dialog Semiconductor DA9063 (U30)	-	Supported
	VCCQ_SD1 (3.3/1.8 V)	Dialog Semiconductor DA9063 (U30)	-	Supported
	VIO33 (3.3 V)	Dialog Semiconductor DA9063 (U30)	-	Supported
	VLDO7_1.8V	Dialog Semiconductor DA9063 (U30)	-	Supported
	VCCQ_SD0 (3.3/1.8V)	Dialog Semiconductor DA9063 (U30)	-	Supported
	SDIF_POWER (3.3 V)	Analog Devices ADP3339AKCZ-3.3R7 (U12, not mounted)	-	Supported

2.18.2. Block Diagram

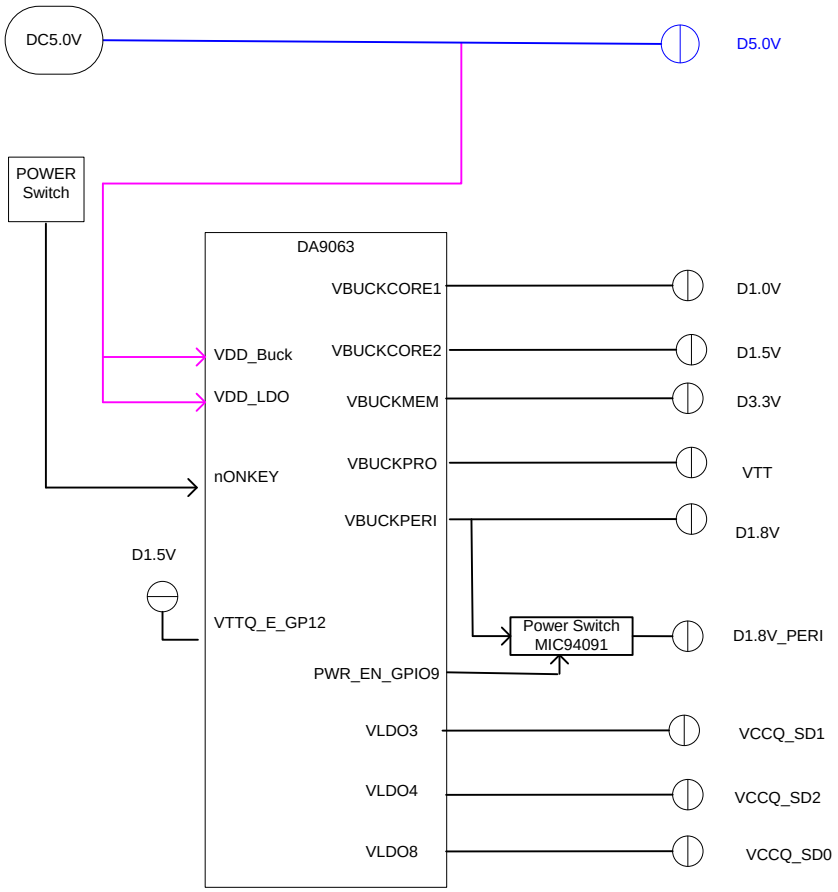
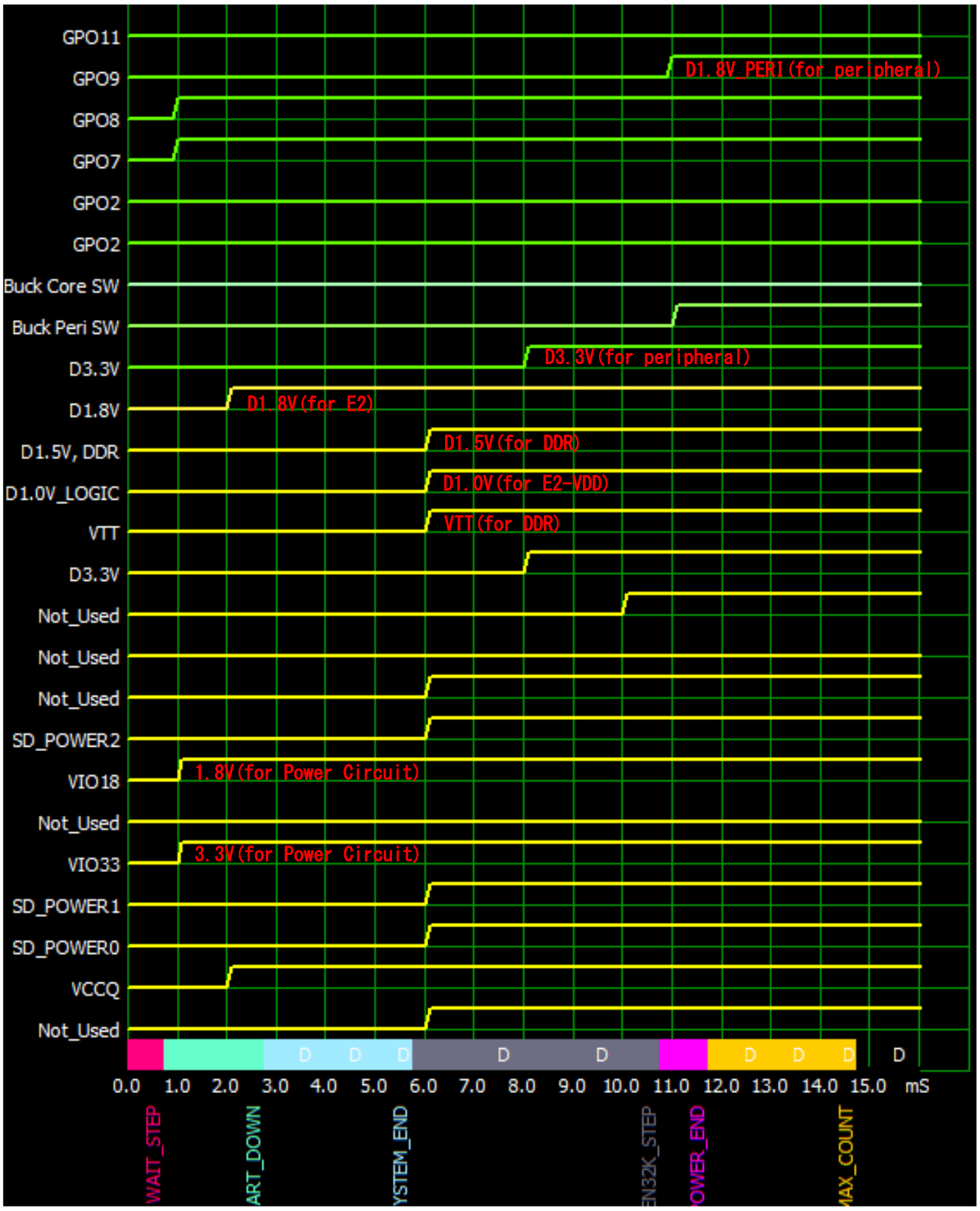


Figure 2.18.1 Block Diagram of Power Supply Circuit

2.18.3. Power Supply Sequencing

The diagram of the sequence for turning on the power (DA9063 OTP) to the YR8A77450HA02BG board is shown below.



Notes:1. In the power-off sequence, turn off the power supplies in reverse order of the power-on sequence.

Figure 2.18.2 Power-On Sequence

2.19. EXIO Connectors (JP1, JP2)

2.19.1. Specifications

The YR8A77450HA02BG board incorporates two connectors (JP1, JP2) that are connected to the peripheral I/O signals of the RZ/G1E. The arrangement of connectors and pins on the YR8A77450HA02BG board is shown below.

Table 2.19.1 EXIO Connector Specification

EXIO Connector (JP1)	Box Wafer 10-pin, 2.0-mm pitch.
EXIO Connector (JP2)	Box Wafer 6-pin, 2.0-mm pitch

Table 2.19.2 List of EXIO Connector (JP1) Pins

Pin	Net Name	Pin	Net Name
1	MSIOF1_SYNC	2	MSIOF1_SCK
3	MD5/MSIOF1_TXD	4	MISOF1_RXD
5	I2C3_SDA_B	6	I2C3_SCL_B
7	GP3_22	8	GP3_30
9	GND	10	GND

Table 2.19.3 List of EXIO Connector (JP2) Pins

Pin	Net Name	Pin	Net Name
1	D3.3V	2	GP1_14/TS_SDATA0_B
3	GP1_16/TS_SDEN0_B	4	GP1_17/TS_SPSYNC0_B
5	GP1_15/TS_SCK0_B	6	GND

3.

3. Outline Diagrams of YR8A77450HA02BG Board

3.1. External Dimensions and Hole Locations of YR8A77450HA02BG Board

The following shows the external dimensions and hole locations of the YR8A77450HA02BG board. (Unit: mm)

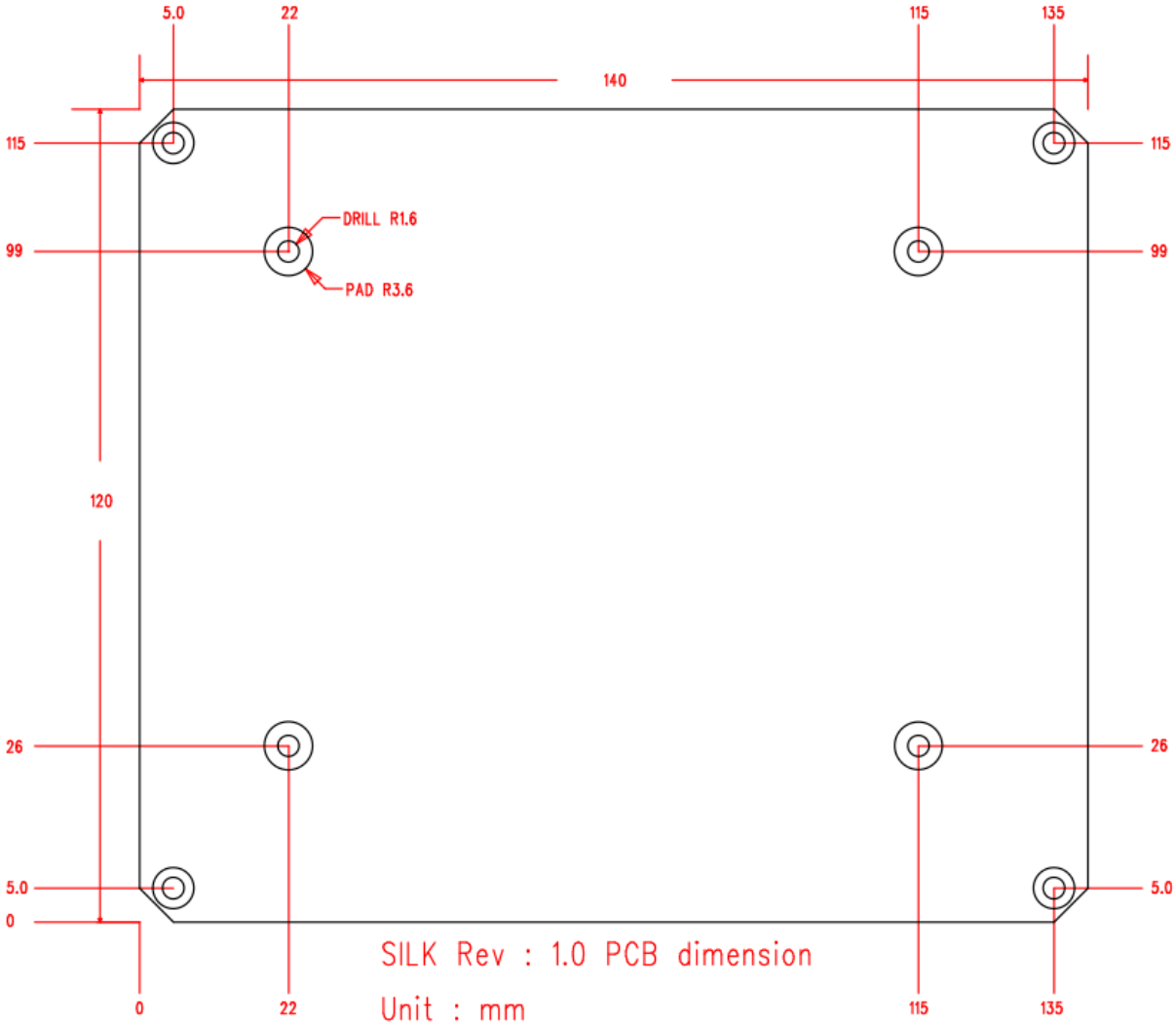


Figure 3.1.1 External Dimensions and Hole Locations of the YR8A77450HA02BG Board (Top View)

3.2. Connector Locations on YR8A77450HA02BG Board (Component Surface)

The following shows the connector locations on the component surface.

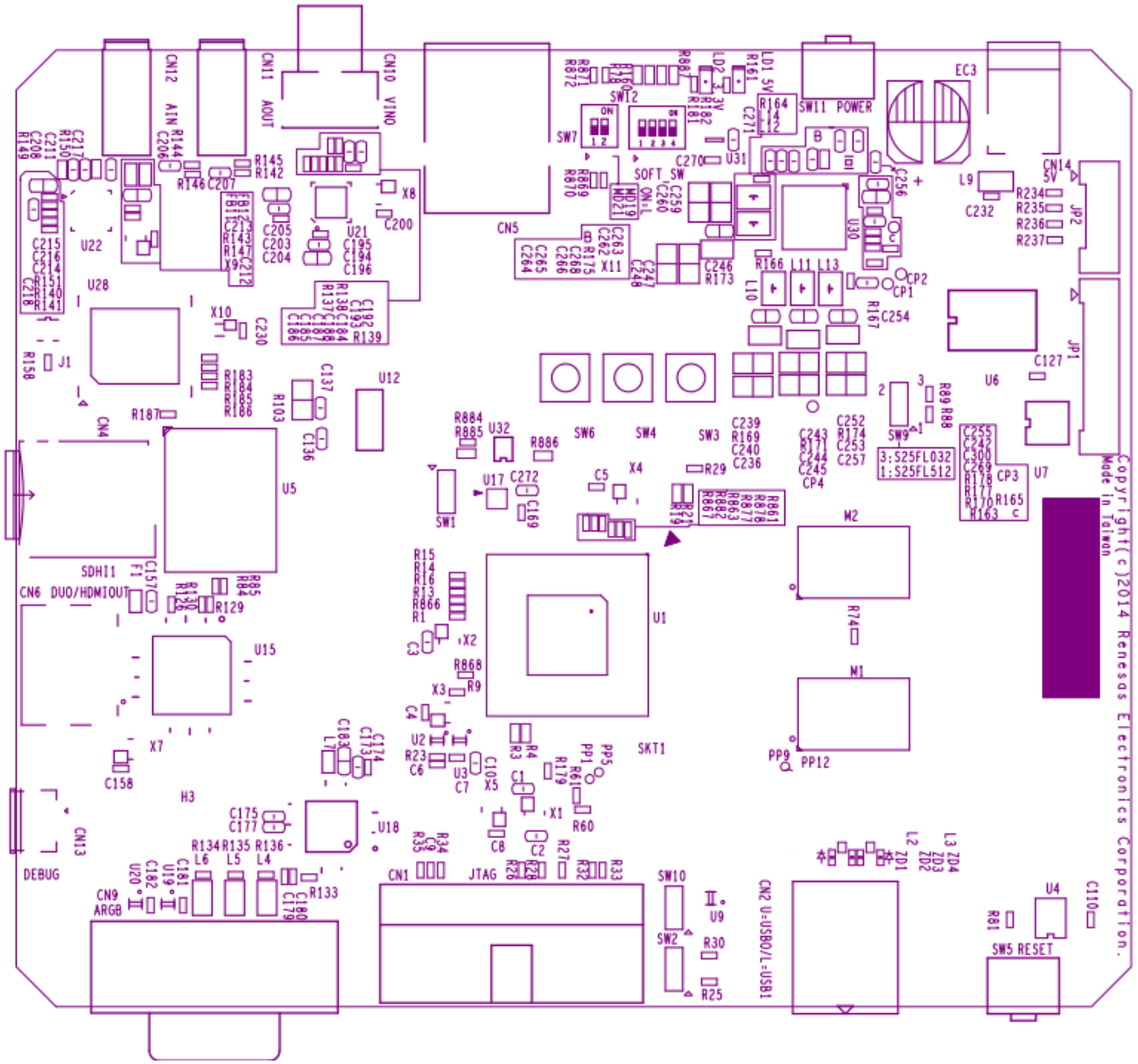


Figure 3.2.1 Connector Locations of the YR8A77450HA02BG Board (Component Surface) (Top View)

3.3. Connector Locations on YR8A77450HA02BG Board (Solder Surface)

The following shows the connector locations on the solder surface.

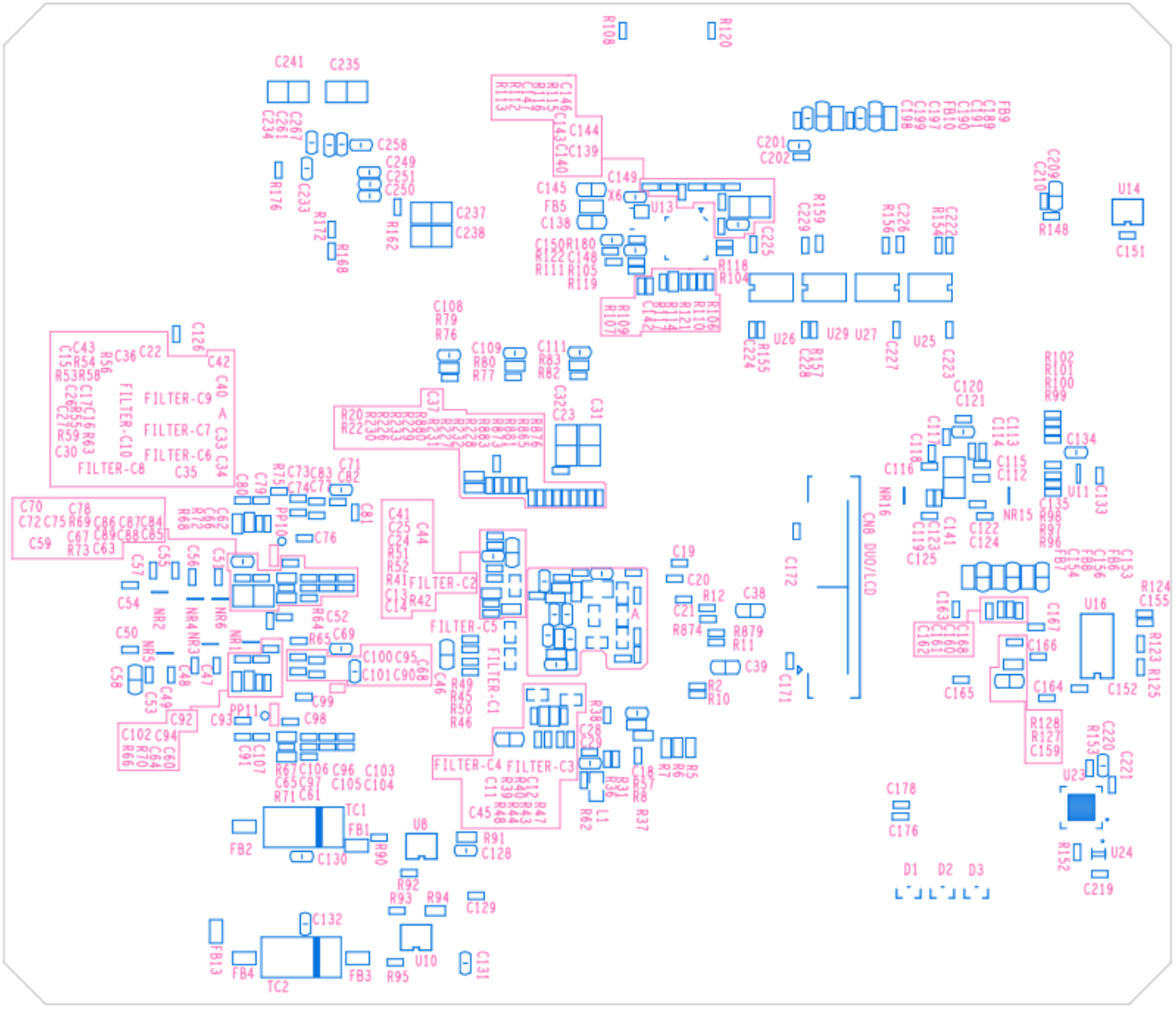


Figure 3.3.1 Connector Locations of the YR8A77450HA02BG Board (Solder Surface) (Top View)

RZ/G1E Starter Kit Board (YR8A77450HA02BG)
Hardware Manual

Publication Date: Rev. 1.00 Oct 2017
Published by:

Renesas Electronics America Co., Ltd.